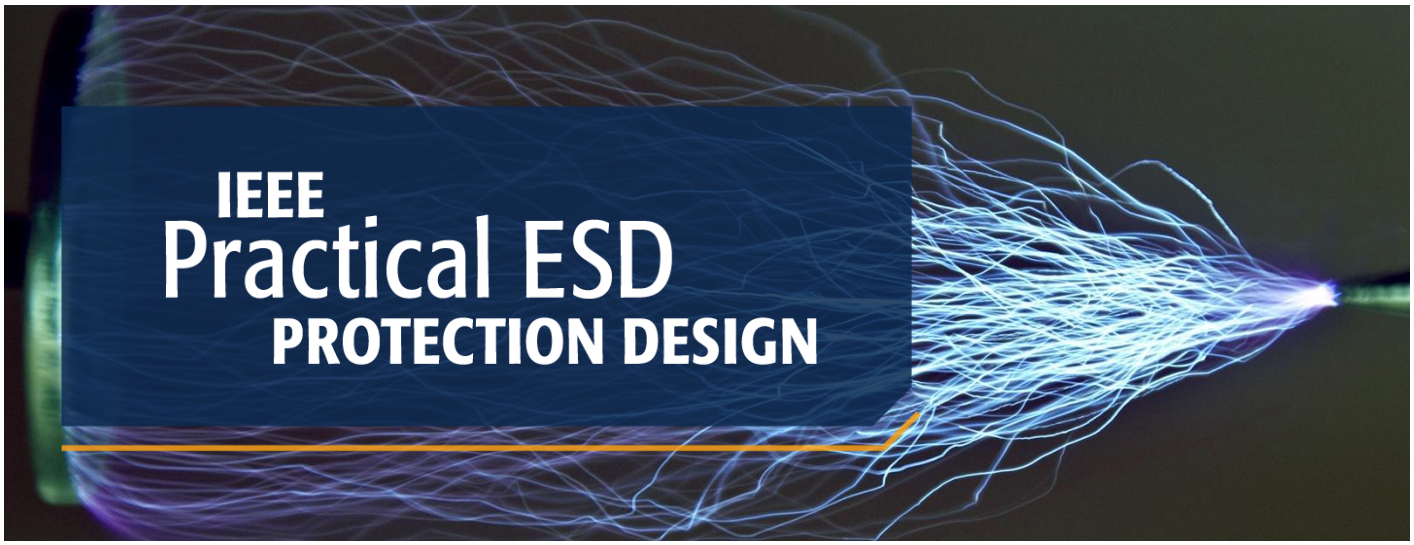

IEEE Practical ESD Protection Design

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Preface

This course provides essential knowledge on Electrostatic Discharge (ESD) Protection in electronic design, covering key concepts such as ESD failure analysis, test models, protection devices, and advanced protection circuits. Topics include the fundamentals of ESD, its effects on integrated circuits, various ESD protection devices (e.g., diodes, MOSFETs, BJTs, SCRs), and full-chip ESD protection techniques. The course also explores emerging solutions like graphene-based ESD protection and the use of TCAD-based simulations for optimizing designs. Additionally, it covers RF and mixed-signal ESD protection, along with CAD tools for design verification. The course emphasizes practical ESD design considerations, including layout techniques, device modeling, and the integration of protection in advanced IC technologies.

This course is designed for engineers and designers involved in integrated circuit design and those seeking to improve their understanding of ESD protection strategies. It assumes that you have a basic background in electronics and IC design. Knowledge of circuit design and semiconductor devices is helpful, but not required.

Lesson 1:

Why ESD?

This lesson emphasizes the importance of understanding and addressing ESD (electrostatic discharge) in modern industries. It begins by providing a historical perspective on ESD, outlining its origins, key milestones, and the growing awareness of its effects on sensitive electronic systems over time. The lesson then explores the dangers of ESD, such as causing irreversible damage to electronic components, disrupting systems, and posing safety hazards. It introduces the fundamental principles of ESD protection, including techniques like grounding, shielding, and charge control, which form the foundation for minimizing ESD risks. Furthermore, it discusses the need to strike a balance between overprotection, which can lead to unnecessary costs, and underprotection, which leaves systems vulnerable. Finally, the lesson highlights how ESD protection methods have evolved from basic approaches to revolutionary advancements, reflecting the industry's ongoing efforts to address new challenges with cutting-edge solutions. This comprehensive overview underscores the critical role of ESD protection in ensuring the reliability and safety of electronic systems.

1.1 A Historical Perspective 00:30 min

Knowledge Check	1 Item	05:00 mm:ss

1.2 ESD and the Dangers 02:00 min

Knowledge Check	3 Items	15:00 mm:ss
Quiz	6 Items	30:00 mm:ss

1.3 ESD Protection: The Principles 01:15 min

Quiz	3 Items	15:00 mm:ss

1.4 ESD Protection: More or Less? 00:45 min

Quiz	1 Item	05:00 mm:ss

1.5 ESD Protection: Evolution to Revolution 00:25 min

Key Terms

Flashcards	10 Items	20:00 mm:ss

Total Lesson Time

Lesson 2:

ESD Failure Analysis

This lesson focuses on ESD Failure Analysis, exploring how Electrostatic Discharge (ESD) impacts electronic systems and components. It defines ESD failure and outlines the criteria for identifying such failures, distinguishing between hard failures (permanent damage) and soft failures (temporary malfunctions). The lesson introduces various techniques for ESD Failure Analysis (FA), emphasizing methods to detect and diagnose issues effectively. It also highlights ESD failure signatures, which are unique patterns indicating damage caused by ESD, and examines soft failures, which can cause intermittent or hidden problems. Additionally, the lesson discusses failure correlation, connecting observed failures to specific ESD events to trace root causes, and explores ESD failure models, which simulate system responses to ESD to design more resilient electronics. This comprehensive overview equips engineers with the knowledge and tools to analyze, predict, and mitigate ESD-related risks in electronic systems.

2.1 ESD Failure Analysis

00:45 min

Topic

- ESD Failure Criteria
- Hard and Soft ESD Failures

Knowledge Check	1 Item	05:00 mm:ss
Quiz	2 Items	10:00 mm:ss

2.2 ESD FA Techniques

00:50 min

Knowledge Check	2 Items	10:00 mm:ss
Quiz	2 Items	10:00 mm:ss

2.3 ESD Failure Signatures

02:35 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	2 Items	10:00 mm:ss

2.4 ESD Soft Failures

00:20 min

2.5 ESD Failure Correlation

00:55 min

Quiz	1 Item	05:00 mm:ss

2.6 ESD Failure Models 00:45 min

Quiz	1 Item	05:00 mm:ss

Key Terms

Flashcards	2 Items	05:00 mm:ss

Total Lesson Time

Lesson 3:

ESD Test Models and Standards

This lesson explores the key ESD test models and standards that help simulate and mitigate the effects of Electrostatic Discharge (ESD) on electronic devices. It begins with an overview of ESD origins and its impact on sensitive components, emphasizing the need for standardized testing. The Human Body Model (HBM) simulates ESD from human contact, while the Machine Model (MM) addresses discharges from machinery in industrial settings. The Charged Device Model (CDM) focuses on rapid discharges from charged components touching grounded surfaces, often causing severe damage. The IEC Model evaluates the robustness of consumer and industrial electronics under real-world ESD scenarios, adhering to international standards, and the Transmission Line Pulse (TLP) Model provides precise analysis of device behavior under ESD stress, identifying failure thresholds. By detailing these models, the lesson underscores their importance in designing ESD-resistant devices and ensuring the reliability of electronic systems in diverse environments.

3.1 ESD Origins 00:45 min

Knowledge Check	2 Items	10:00 mm:ss
Quiz	1 Item	05:00 mm:ss

3.2 HBM Model 01:30 min

Quiz	1 Item	05:00 mm:ss

3.3 MM Model 00:55 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	2 Items	10:00 mm:ss

3.4 CDM Model 01:20 min

Quiz	2 Items	10:00 mm:ss

3.5 IEC Model 00:50 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	1 Item	05:00 mm:ss

3.6 TLP Model 01:00 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	2 Items	10:00 mm:ss

3.7 Summary 00:20 min

Key Terms

Flashcards	5 Items	10:00 mm:ss

Total Lesson Time

Lesson 4:

ESD Protection Devices

This lesson provides an in-depth exploration of ESD protection devices and mechanisms, focusing on the technologies used to safeguard electronic systems against Electrostatic Discharge (ESD). It begins with on-chip ESD protection mechanisms and the role of switches in discharging ESD safely. The lesson examines the differences between active and passive ESD protection, emphasizing their respective applications. It dives into the use of diodes, covering their physics, role in ESD protection, and parasitic modeling. Similarly, it explains the use of BJTs (Bipolar Junction Transistors) and MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) for ESD protection, exploring their device physics, implementation, and parasitic modeling, with a specific focus on ggMOS (gate-grounded MOSFETs) for enhanced protection. Additionally, SCRs (Silicon-Controlled Rectifiers) are discussed for their high-current handling capability, including their physics, implementation, and parasitic modeling in ESD applications. Through detailed explanations of these devices and their roles, the lesson highlights the evolution of ESD protection technologies and their critical importance in ensuring the reliability of modern electronic systems.

4.1 On-Chip ESD Protection Mechanisms

Topic

02:05 min

- Switch for ESD Discharge
- ESD Protection: Active versus Passive

Knowledge Check	2 Items	10:00 mm:ss
Quiz	5 Items	25:00 mm:ss

4.2 Diode for ESD Protection

Topic

01:10 min

- Diode Device Physics
- Diode in ESD Protection
- Diode ESD Parasitic Modeling

Knowledge Check	1 Item	05:00 mm:ss
Quiz	3 Items	15:00 mm:ss

4.3 BJT for ESD Protection

Topic

01:00 min

- BJT Device Physics
- BJT in ESD Protection
- BJT ESD Parasitic Modeling

Quiz	1 Item	05:00 mm:ss

4.4 MOSFET for ESD Protection

Topic

01:10 min

- MOSFET Device Physics
- ggMOS in ESD Protection
- MOSFET ESD Parasitic Modeling

Knowledge Check	1 Item	05:00 mm:ss

4.5 SCR for ESD Protection

Topic

01:35 min

- SCR Device Physics
- SCR in ESD Protection
- SCR ESD Parasitic Modeling

Knowledge Check	1 Item	05:00 mm:ss
Quiz	1 Item	05:00 mm:ss

4.6 Summary

00:15 min

Key Terms

Flashcards	4 Items	10:00 mm:ss

Total Lesson Time

Lesson 5:

ESD Protection Circuits

This lesson focuses on the design and implementation of ESD protection circuits, which are essential for safeguarding electronic devices against Electrostatic Discharge (ESD). It begins with I/O ESD protection, ensuring robust defenses at input and output terminals, and introduces two-stage ESD protection for enhanced reliability. Multiple-finger ESD protection is explored for handling high currents, while specific circuits for MOSFETs, BJTs, and SCRs are discussed, highlighting their unique roles and applications. The lesson also emphasizes ESD self-protection, where components are designed to protect themselves during ESD events, and explores output ESD protection for safe signal transmission. Advanced concepts like low-triggering ESD protection circuits and various types of ESD power clamps—including diode-string, MOSFET, SCR, and any-switch power clamps—are analyzed for their ability to control voltage surges and safeguard power lines. Through these discussions, the lesson underscores the importance of tailored circuit designs in building reliable, ESD-resilient electronic systems.

5.1 I/O ESD Protection

Topic

02:25 min

- Two-Stage ESD Protection
- Multiple-Fingers ESD Protection
- MOSFET ESD Protection Circuits
- BJT ESD Protection Circuits
- SCR ESD Protection Circuits

Knowledge Check	2 Items	10:00 mm:ss
Quiz	3 Items	15:00 mm:ss

5.2 ESD Self-Protection

Topic

01:00 min

- Output ESD Protection
- ESD Self-Protection

Knowledge Check	1 Item	05:00 mm:ss
Quiz	2 Items	10:00 mm:ss

5.3 Low-Triggering ESD Protection Circuits

01:05 min

Knowledge Check	1 Item	04:00 mm:ss
Quiz	2 Items	10:00 mm:ss

5.4 ESD Power Clamps

Topic

01:35 min

- Diode-String Power Clamps
- MOSFET Power Clamps
- SCR Power Clamps
- Any Switch Power Clamps

	Knowledge Check	2 Items	10:00 mm:ss
	Quiz	4 Items	20:00 mm:ss

5.5

Summary

00:15 min

Key Terms

	Flashcards	6 Items	15:00 mm:ss

Total Lesson Time

Lesson 6:

Full-Chip ESD Protection

This lesson provides an in-depth examination of Full-Chip ESD Protection, focusing on the strategies and principles used to safeguard entire semiconductor chips from the damaging effects of Electrostatic Discharge (ESD). It begins by outlining the fundamental principles of full-chip protection, introducing the concept of the ESD protection design window, which defines the optimal range for implementing protection circuits without compromising performance. The lesson delves into advanced ESD protection, emphasizing the objective of achieving high levels of protection with minimal additional circuitry to maintain efficiency and cost-effectiveness. It further explores the need for dual-polarity ESD protection to protect against both positive and negative discharges and multiple-polarity protection for more complex and sophisticated systems. The discussion then shifts to various full-chip ESD protection schemes, including the pad-clamp scheme for protecting individual I/O pads and the global ESD bus scheme, which integrates protection across the entire chip. Lastly, the lesson stresses that there is no one-size-fits-all solution to ESD protection, as different applications and environments require tailored approaches to meet their unique challenges, ensuring robust and reliable chip performance under ESD conditions.

6.1 Full-Chip ESD Protection Principles

00:45 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	2 Items	10:00 mm:ss

6.2 ESD Protection Design Window

00:35 min

Knowledge Check	1 Item	05:00 mm:ss

6.3 Advanced ESD Protection: More at Less

Topic

01:45 min

- Dual-Polarity ESD Protection
- Multiple-Polarity ESD Protection

Quiz	3 Items	15:00 mm:ss

6.4 Full-Chip ESD Protection Schemes

Topic

01:10 min

- Full-Chip ESD Consideration
- Pad-Clamp Scheme
- Global ESD Bus Scheme

Knowledge Check	1 Item	05:00 mm:ss
Quiz	2 Items	10:00 mm:ss

6.5 No Universal ESD Protection Solution

00:25 min

Quiz	1 Item	05:00 mm:ss

Key Terms

Flashcards	4 Items	10:00 mm:ss

Total Lesson Time

Lesson 7:

Mixed-Signal and HV ESD Protection

This lesson provides a comprehensive exploration of ESD protection techniques for Mixed-Signal ICs and High-Voltage ICs, which present unique challenges due to their complex operating environments. It begins by detailing the specific ESD protection requirements for Mixed-Signal ICs, which integrate both analog and digital components on a single chip. These ICs need protection strategies that account for the potential interference between the analog and digital sections during an ESD event. The lesson also delves into ESD protection for multiple-voltage ICs, where circuits operate at different voltage levels, requiring a delicate balance in protection design to accommodate each voltage's requirements without affecting the circuit's functionality. It then discusses high-voltage ICs, which are exposed to higher energy discharges, necessitating robust and advanced protection mechanisms. A key focus is on ensuring ESD design window compliance, meaning that protection circuits must provide sufficient shielding against ESD without compromising the performance of the IC. The lesson also emphasizes the critical importance of latch-up immunity, where improper handling of ESD can lead to latch-up conditions, causing permanent damage or failure of the device. Finally, the lesson highlights that tailored, specific ESD protection strategies are required for each type of IC, taking into account factors such as voltage levels, signal integrity, and the overall operational environment to maintain both reliability and performance under real-world conditions.

7.1 ESD Protection for Mixed-Signal ICs

01:30 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	4 Items	20:00 mm:ss

7.2 ESD Protection for Multiple-Voltages ICs

01:20 min

Knowledge Check	3 Items	15:00 mm:ss
Quiz	2 Items	10:00 mm:ss

7.3 ESD Protection for High-Voltage ICs

Topic

02:10 min

- ESD Design Window Compliance
- Latch-up Immunity

Knowledge Check	2 Items	10:00 mm:ss
Quiz	1 Item	05:00 mm:ss

7.4 Summary

00:10 min

Key Terms

Flashcards	5 Items	10:00 mm:ss

Total Lesson Time

Lesson 8:

TCAD-Based Mixed-Mode ESD Protection Designs

This lesson provides an in-depth exploration of TCAD-based mixed-mode ESD protection designs, showcasing how Technology Computer-Aided Design (TCAD) simulations are integral to optimizing and predicting the effectiveness of ESD protection circuits in complex, mixed-mode electronic systems. The lesson begins by explaining the importance of ESD design optimization and prediction, focusing on how TCAD simulations can model ESD events and help engineers refine their designs to minimize damage. It introduces the TCAD-based mixed-mode ESD simulation-design methodology, which combines both analog and digital design aspects to accurately simulate real-world conditions. The lesson includes practical examples, such as understanding basic TCAD ESD simulations, comparing ggNMOS and gcNMOS ESD protection types, and analyzing ESD power clamp designs in 0.35 µm CMOS technology, which is often used in mixed-signal ICs. Further, it covers high-voltage ESD protection design optimization, illustrating how to fine-tune circuits to withstand higher energy discharges. Additional case studies involve advanced 3D TCAD layout analysis, which allows for a more comprehensive understanding of how physical geometry affects ESD performance, and multiple-stimuli TCAD ESD simulations, used to simulate varying real-world conditions to ensure the resilience of protection circuits. Through these practical

examples, the lesson demonstrates how TCAD tools enable engineers to design and refine ESD protection systems that are both effective and efficient, reducing the risk of device failure due to electrostatic discharge in real-world applications.

8.1 ESD Design Optimization and Prediction

01:45 min

Knowledge Check	3 Items	15:00 mm:ss
Quiz	4 Items	20:00 mm:ss

8.2 TCAD-Based Mixed-Mode ESD Simulation-Design Methodology

01:55 min

Knowledge Check	2 Items	10:00 mm:ss
Quiz	3 Items	15:00 mm:ss

8.3 Mixed-Mode ESD Simulation-Design Examples

04:10 min

Topic

- Example 1: Understand TCAD ESD Simulation
- Example-2: ggNMOS versus gcNMOS ESD Protection
- Example-3: ESD Power Clamp in 0.35 µm CMOS

Knowledge Check	4 Items	20:00 mm:ss
Quiz	3 Items	15:00 mm:ss

- Example-4: Optimize HV ESD Protection Design
- Example-5: ESD Layout Analysis by 3D TCAD
- Example-6: Multiple-Stimuli TCAD ESD Simulation

8.4 Summary

00:15 min

Key Terms

Flashcards	7 Items	15:00 mm:ss

Total Lesson Time

Lesson 9:

RF ESD Protection

This lesson delves into the specific challenges of RF ESD protection, which is essential for safeguarding radio frequency (RF) circuits that are particularly sensitive to electrostatic discharge (ESD) due to their high-frequency operation. It starts by addressing what makes RF ESD protection special, emphasizing that RF circuits require protection solutions that minimize parasitic elements—such as capacitance and inductance—that could distort or degrade signal quality, thereby affecting the overall performance. The lesson highlights the need for careful RF ESD protection characterization, explaining how engineers assess the effectiveness of protection circuits in RF applications, ensuring that they don't interfere with the delicate signal transmission. Special focus is given to low-parasitic ESD protection solutions, which are designed to offer robust protection without compromising the RF signal integrity. Through a detailed RF ESD protection design example, the lesson demonstrates how these protection techniques can be practically applied, showing the balance between providing adequate protection and maintaining the quality of RF performance. By addressing these unique challenges, the lesson underscores the importance of designing ESD protection circuits that meet the high standards required for RF applications while ensuring the devices remain durable and functional under ESD stress.

9.1 What Is Special for RF ESD Protection? 01:30 min

Knowledge Check	4 Items	20:00 mm:ss
Quiz	2 Items	10:00 mm:ss

9.2 RF ESD Protection Characterization 01:15 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	3 Items	15:00 mm:ss

9.3 Low-Parasitic ESD Protection Solutions 00:35 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	3 Items	15:00 mm:ss

9.4 RF ESD Protection Design Example 00:20 min

9.5 Summary 00:15 min

Key Terms

Flashcards	5 Items	15:00 mm:ss

Total Lesson Time

Lesson 10:

ESD-RFIC Co-Design

This lesson dives deeply into the intricate relationship between ESD protection and RFIC (Radio Frequency Integrated Circuit) design, emphasizing the mutual influence each has on the other in high-frequency applications. It begins by discussing ESD-IC interactions, highlighting how the design of ESD protection circuits can impact the functionality and performance of RFICs, which are particularly sensitive to parasitic elements like capacitance and inductance that could disrupt signal integrity. Similarly, the lesson explores how the presence of ESD protection can sometimes affect the overall performance of the IC, especially in high-speed or RF systems. The core concept of ESD-RFIC co-design is introduced, emphasizing that a holistic design approach that considers both ESD protection and RFIC performance together is essential for optimizing system reliability without compromising functionality. The ESD-RFIC co-design principle is detailed, demonstrating how to harmonize the protection mechanisms with the high-frequency needs of the circuit. Several ESD-RFIC co-design examples are provided to showcase how engineers balance these factors in practice, ensuring that ESD protection does not degrade the RF signal and that both components work together seamlessly. The lesson concludes by reinforcing the critical importance of integrating ESD protection strategies early in the RFIC design process to maintain system robustness, performance, and reliability across all operating conditions.

10.1 ESD-IC Interactions

Topic

01:55 min

- IC Affects ESD Protection
- ESD Affects IC Performance

Knowledge Check	2 Items	10:00 mm:ss
Quiz	4 Items	20:00 mm:ss

10.2 ESD-RFIC Co-Design

Topic

01:55 min

- ESD-RFIC Co-Design Principle
- ESD–RFIC Co-Design Examples

Knowledge Check	2 Items	10:00 mm:ss
Quiz	2 Items	10:00 mm:ss

10.3 Summary

00:15 min

Key Terms

Flashcards	5 Items	10:00 mm:ss

Total Lesson Time

Lesson 11:

ESD Layout Designs

This lesson focuses on the critical role of layout design in ESD protection for integrated circuits, outlining how the physical layout of components can dramatically influence the performance of protection circuits against electrostatic discharge. It starts by highlighting that layout is critical to ESD protection because the way components are arranged can either enhance or compromise a circuit's ability to withstand ESD events. The lesson explores basic ESD protection layout, discussing simple, foundational design strategies that ensure effective initial protection, and moves on to advanced ESD protection layout techniques that address more complex scenarios, such as higher energy levels or intricate circuit architectures. Further, the lesson dives into advanced ESD layout considerations, where careful attention to factors like parasitic capacitance, inductance, and current paths is necessary to prevent damage and maintain circuit performance. It emphasizes that ESD design layout is an art, requiring a deep understanding of both electrical principles and practical design trade-offs to balance ESD protection with factors like signal integrity and overall system performance. The lesson also introduces 3D TCAD simulations as a powerful tool for visualizing and optimizing ESD layouts, offering detailed insights into how different layouts affect ESD behavior and circuit resilience. By incorporating these simulation tools, engineers can refine their designs to ensure maximum protection while minimizing the impact on device performance. The lesson concludes by stressing that a well-executed layout design is essential for creating reliable, durable circuits that can effectively handle ESD events without compromising functionality.

11.1 Layout is Critical to ESD Protection

00:55 min

Knowledge Check	2 Items	10:00 mm:ss
Quiz	3 Items	15:00 mm:ss

11.2 Basic ESD Protection Layout

02:05 min

Knowledge Check	4 Items	20:00 mm:ss
Quiz	4 Items	20:00 mm:ss

11.3 Advanced ESD Protection Layout

Topic

01:45 min

- Advanced ESD Layout Considerations
- ESD Design Layout is an Art

Knowledge Check	1 Item	05:00 mm:ss
Quiz	4 Items	20:00 mm:ss

11.4 3D TCAD for ESD Layout Designs

01:10 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	1 Item	05:00 mm:ss

11.5

Summary 00:10 min

Key Terms

Flashcards	4 Items	10:00 mm:ss

Total Lesson Time

Lesson 12:

ESD versus IC Technologies

This lesson explores the relationship between ESD protection and various IC technologies, emphasizing how advances in semiconductor technologies impact the design and effectiveness of ESD protection circuits. It begins by discussing how IC technologies influence ESD protection, highlighting the challenges posed by smaller geometries and more complex materials in modern IC designs. The lesson covers the role of ESD metal interconnects, which are essential for managing current during an ESD event, and how their properties affect the overall ESD protection strategy. It introduces the concept of technology-ESD co-development, where ESD protection is considered alongside IC technology development to ensure seamless integration. A specific focus is placed on graphene heat spreading, a cutting-edge material that offers promising solutions for managing heat in advanced ICs, potentially improving their ESD performance. The lesson also explores how technology affects the ESD design window, with newer technologies often leading to tighter ESD protection requirements. Finally, it questions whether lowering ESD protection for advanced ICs is a viable approach, given the trade-offs in performance, cost, and reliability. The lesson concludes by highlighting the need for a holistic approach to ESD protection that takes into account evolving IC technologies to maintain system robustness.

12.1 IC Technologies and ESD Protection

02:15 min

Topic

- ESD Metal Interconnects
- Technology-ESD Co-Development
- Graphene Heat Spreading

Knowledge Check	3 Items	15:00 mm:ss
Quiz	7 Items	35:00 mm:ss

12.2 Technology Affects ESD Design Window

00:25 min

Quiz	2 Items	10:00 mm:ss

12.3 Lowering ESD Protection for Advanced ICs?

00:40 min

Quiz	2 Items	10:00 mm:ss

12.4 Summary

00:15 min

Key Terms

Flashcards	2 Items	05:00 mm:ss

Total Lesson Time

Lesson 13:

ESD Circuit Simulation by SPICE

This lesson focuses on the use of SPICE (Simulation Program with Integrated Circuit Emphasis) for ESD circuit simulation, which plays a crucial role in designing and verifying ESD protection circuits. It begins by explaining ESD device behavior modeling, where SPICE is used to simulate the behavior of individual ESD protection devices, helping engineers predict how they will respond to electrostatic discharge events. The lesson explores full-chip ESD circuit simulation by SPICE, demonstrating how entire integrated circuits, including their protection mechanisms, can be modeled and tested for ESD resilience. The principles for ESD circuit simulation by SPICE are discussed, emphasizing the need to accurately model the physical characteristics of devices and interconnects in order to simulate real-world conditions effectively. Finally, the lesson covers circuit-level ESD design verification by SPICE, explaining how SPICE simulations are used to verify that ESD protection circuits meet required standards and perform reliably under various ESD scenarios. The lesson concludes by reinforcing the importance of SPICE simulations in ensuring the effectiveness and reliability of ESD protection strategies throughout the design process.

13.1 ESD Device Behavior Modeling 01:15 min

Knowledge Check	2 Items	10:00 mm:ss
Quiz	3 Items	15:00 mm:ss

13.2 Full-Chip ESD Circuit Simulation by SPICE

Topic

02:30 min

- Principle for ESD Circuit Simulation by SPICE
- Circuit-Level ESD Design Verification by SPICE

Knowledge Check	5 Items	25:00 mm:ss
Quiz	7 Items	35:00 mm:ss

13.3 Summary 00:10 min

Key Terms

Flashcards	3 Items	05:00 mm:ss

Total Lesson Time

Lesson 14:

Emerging ESD Protection

This lesson explores emerging ESD protection technologies that are addressing the increasing challenges posed by modern, miniaturized electronic devices. It begins by identifying the emerging ESD protection challenges, which are driven by the need for more compact, efficient, and higher-performance protection solutions due to the shrinking sizes of integrated circuits and the increasing complexity of modern designs. The lesson then covers dispensable ESD protection, which refers to protection methods that can be applied in a flexible, temporary, or on-demand manner, offering convenience and adaptability. It introduces field-programmable ESD protection, where protection circuits can be customized or reconfigured in the field to meet evolving requirements. The lesson also explores nano-crystal quantum-dots ESD protection, a cutting-edge technology that leverages the unique properties of quantum dots to enhance the efficiency and reliability of ESD protection. Another emerging method discussed is SONOS ESD protection, which uses Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) structures to provide high-performance ESD protection in advanced ICs. Additionally, the lesson touches on interposer/TSV-based ESD protection, which involves using interposers and through-silicon vias (TSVs) to manage ESD events in 3D integrated circuits. The lesson concludes by summarizing how these emerging technologies are

shaping the future of ESD protection, providing more effective, scalable, and adaptable solutions to meet the demands of next-generation electronics.

14.1 Emerging ESD Protection Challenges

00:20 min

Knowledge Check	1 Item	05:00 mm:ss

14.2 Dispensable ESD Protection

01:15 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	5 Items	25:00 mm:ss

14.3 Field-Programmable ESD Protection

Topic

- Nano-Crystal Quantum-Dots ESD Protection
- SONOS ESD Protection

00:45 min

Quiz	1 Item	05:00 mm:ss

14.4 Interposer/TSV-Based ESD Protection 01:05 min

	Knowledge Check	1 Item	05:00 mm:ss
	Quiz	4 Items	20:00 mm:ss

14.5 Summary 00:15 min

Key Terms

	Flashcards	4 Items	10:00 mm:ss

Total Lesson Time

Lesson 15:

ESD CAD for Full-Chip Design Verification

This lesson delves into the critical role of CAD (Computer-Aided Design) tools in full-chip ESD design verification, which is essential for ensuring that integrated circuits are robust against electrostatic discharge (ESD) events that could otherwise lead to failure. It starts by explaining the process of full-chip ESD design verification, which involves simulating the behavior of the entire integrated circuit to ensure that each component and interconnect is adequately protected against ESD threats. The lesson emphasizes how CAD algorithms for ESD design verification automate the detection and analysis of potential vulnerabilities in the chip design, streamlining the process and improving accuracy. By utilizing these algorithms, designers can quickly and efficiently evaluate whether the ESD protection mechanisms will perform as intended under real-world conditions. Additionally, the lesson presents full-chip ESD design verification examples, showcasing how these tools are applied in practice to validate protection schemes in complex, high-performance chips. These examples demonstrate how CAD tools help identify design flaws early in the development process, which is critical for avoiding costly rework after manufacturing. The lesson concludes by stressing that ESD CAD tools are indispensable for modern chip design, enabling engineers to verify ESD protection comprehensively and efficiently, thus ensuring that the final product is both reliable and resilient to ESD-related failures.or your organization to be secure, it must incorporate security in its day-to-day activities

15.1 Full-Chip ESD Design Verification 00:35 min

Quiz	2 Items	10:00 mm:ss

15.2 CAD Algorithms for ESD Design Verification 02:05 min

Knowledge Check	2 Items	10:00 mm:ss
Quiz	6 Items	30:00 mm:ss

15.3 Full-Chip ESD Design Verification Examples 02:00 min

Knowledge Check	3 Items	15:00 mm:ss
Quiz	2 Items	10:00 mm:ss

15.4 Summary 00:15 min

Key Terms

Flashcards	4 Items	10:00 mm:ss

Total Lesson Time

Lesson 16:

New CDM ESD Protection

This lesson explores new developments in CDM (Charged Device Model) ESD protection, which is essential for protecting electronic devices from ESD events that occur when the device itself is charged. It begins by addressing common misconceptions in CDM ESD protection, highlighting how misunderstandings can lead to inadequate protection designs and failures in real-world applications. The lesson then examines analyzing pad-based CDM ESD protection, which focuses on the importance of designing effective protection at the device's input/output pads, where ESD events are most likely to occur. The lesson also discusses internally distributed CDM ESD protection, which involves distributing protection elements within the chip itself to provide more comprehensive protection across different regions of the circuit. This approach aims to improve the overall robustness of the IC by addressing potential vulnerabilities in both external and internal components. The lesson concludes by summarizing the evolving strategies in CDM ESD protection, stressing the importance of adapting to new insights and techniques to ensure devices remain protected against ESD events in an increasingly complex and miniaturized electronic landscape.

16.1 Misconception in CDM ESD Protection

01:05 min

Knowledge Check	2 Items	10:00 mm:ss
Quiz	2 Items	10:00 mm:ss

16.2 Analyzing Pad-Based CDM ESD Protection

02:05 min

Quiz	4 Items	20:00 mm:ss

16.3 Internally Distributed CDM ESD Protection

00:40 min

Quiz	1 Item	05:00 mm:ss

16.4

Summary

00:10 min

Key Terms

Flashcards	3 Items	10:00 mm:ss

Total Lesson Time

Lesson 17:

Future ESD Protection Outlook

This lesson delves into the future of ESD protection, exploring advanced materials and innovative techniques aimed at overcoming the traditional challenges in safeguarding electronic devices from electrostatic discharge. It begins by addressing the fundamental ESD protection problem, which revolves around designing reliable and efficient protection mechanisms that can withstand the increasing complexity and miniaturization of modern integrated circuits. One key focus is on the above-IC nano-crossbar array ESD switch, a cutting-edge concept that uses nanoscale structures to create high-performance, highly efficient ESD protection switches directly above the IC surface, potentially offering a breakthrough in protecting small-scale components. The

lesson also emphasizes the potential of graphene-based ESD protection switches—taking advantage of graphene's superior electrical conductivity and strength to create faster, more durable protection devices that can perform under more extreme conditions. Graphene ESD protection interconnects are discussed as another promising solution, with graphene's unique properties enhancing the resilience and conductivity of interconnects, ensuring they can handle ESD events without failure. The lesson concludes by reflecting on the future outlook of ESD protection, considering how these advanced materials and design strategies will play a key role in shaping the next generation of electronics. The anticipated developments in graphene-based technologies, nano-structured solutions, and innovative ESD switch designs hold the promise of more compact, cost-effective, and robust protection mechanisms that will be crucial as devices continue to shrink and become more complex.

17.1 The Fundamental ESD Protection Problem

00:35 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	2 Items	10:00 mm:ss

17.2 Above-IC Nano-Crossbar Array ESD Switch

00:40 min

Quiz	1 Item	05:00 mm:ss

17.3 Graphene ESD Protection Switch 00:35 min

Knowledge Check	1 Item	05:00 mm:ss
Quiz	1 Item	05:00 mm:ss

17.4 Graphene ESD Protection Interconnects 00:35 min

Quiz	1 Item	05:00 mm:ss

17.5 Future ESD Protection Outlook 00:20 min

Quiz	1 Item	05:00 mm:ss

17.6 Summary 00:30 min

Key Terms

Flashcards	5 Items	10:00 mm:ss

Total Lesson Time

Approximate Time for the Course

The total time for the course is approximately **89 hours** and **25 minutes**. The time is the sum of the approximate time for each section, calculated using the following:

- **18** Lessons
- **53** Topics
- **153** Quiz
- **78** Flashcards
- **82** Knowledge checks

Total Course Time: **89 hours** and **25 minutes**